MEMS Based Optical Beam Steering System with Applications in Quantum Information Processing

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Abstract

In an effort to create a scalable ion trap quantum architecture, a micro-electro-mechanical (MEMS) based optical beam steering system has been developed to provide individual addressability of an array of trapped atoms. This optical system is used to guide laser beams to address specific locations in that array using MEMS mirrors. These mirrors are able to tilt along one axis with an applied voltage, and this tilt is converted to a lateral shift via optics. By characterizing the different physical parameters of the mirrors, we have been able to optimize the design for optical characteristics, speed, reliability, and manufacturability.

In addition, I have been involved the implementation and integration of the full MEMS system. Due to the specific application for our system, the control electronics required are highly specialized. Using an FPGA based platform, I have been developing a custom scalable control system capable of meeting both the voltage and speed requirements for mirror control, as well as other applications. This system, consisting of a computer based interface, actuation electronics, and high voltage amplifiers, will allow for a multiple beam system to conduct an experiment on a real-time level.

Introduction

Quantum computers have the potential to speed up computation for a number of problems, the classic examples being factorization and cryptography. One potential implementation uses trapped atoms as qubits, with quantum information being stored in the electrical states of each atom. I have, over the past two years in conjunction with Dr. Jungsang Kim, been involved in the development of a micro-electro-mechanical systems (MEMS) based architecture to improve the scalability of ion trap quantum information processing.

In ion trap architectures, lasers are used to manipulate and read qubits. In order to address an array of atoms, we must be able to shift the laser beams to different physical locations corresponding to the atom locations. To achieve this optical shift, a MEMS system consisting of tilting mirrors are used. These mirrors must be fast, reliable, controllable, and must be of high optical quality.[1]

The mirrors are fabricated by either MEMSCAP via the polyMUMPS[2] process, or more recently Sandia's SUMMiT[3] process. These processes allow us to fabricate complex multi-level polysilicon designs. The mirrors are circular and suspended at two points by mechanical springs, allowing for tilt along one axis. The tilt is achieved through electrostatic force; the applied voltage at one of the electrodes induces an attractive force between the electrode and the mirror plate. The mirror plate is coated in a reflective metal (Gold, silver, or aluminum) to minimize optical losses at each mirror. Shown in Figure 1 is the basic physical design of the mirrors.

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[1] See C. Knoernschild, C. Kim, F. P. Lu and J. Kim, Multiplexed Broadband Beam Steering System utilizing High Speed MEMS Mirrors, Optics Express 17, pp 7233 (2009): http://arxiv.org/abs/0902.1574v1 (2009).

[2] See http://www.memscap.com/en_mumps.html for more information

[3] See http://mems.sandia.gov/tech-info/summit-v.html for more information

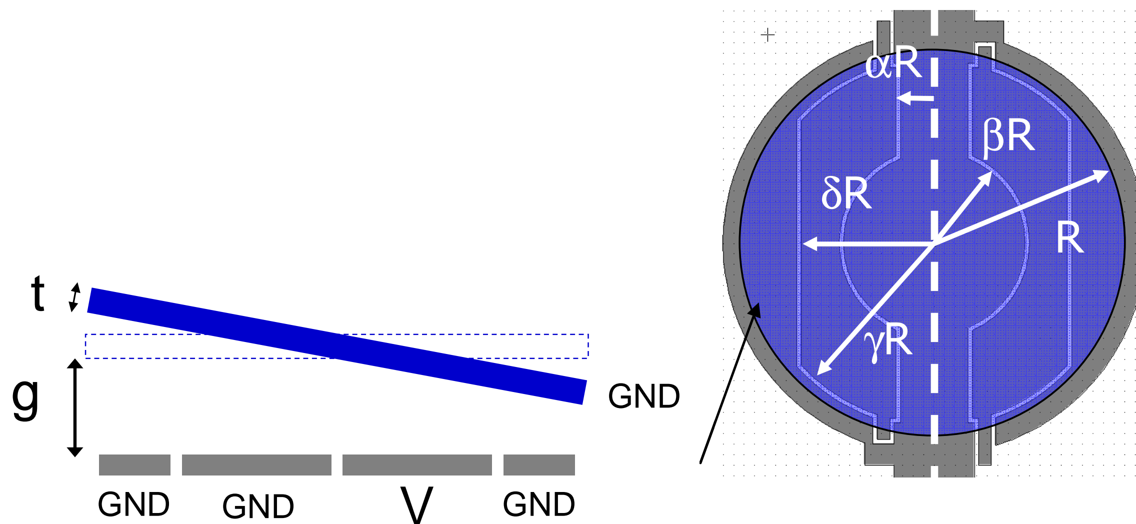

Figure 1 : MEMS Mirror Physical Design. A side view is shown on the left, and a top view on the right. Image courtesy of Caleb Knoernschild

The MEMS mirrors are arranged in an optical system that uses two mirrors to tilt the incoming beam in two orthogonal planes, which is later converted into a lateral shift by means of a lens. By adjusting the tilt, we may adjust the lateral shift, thus allowing different lattice locations to be addressed, as shown in Figure 2.

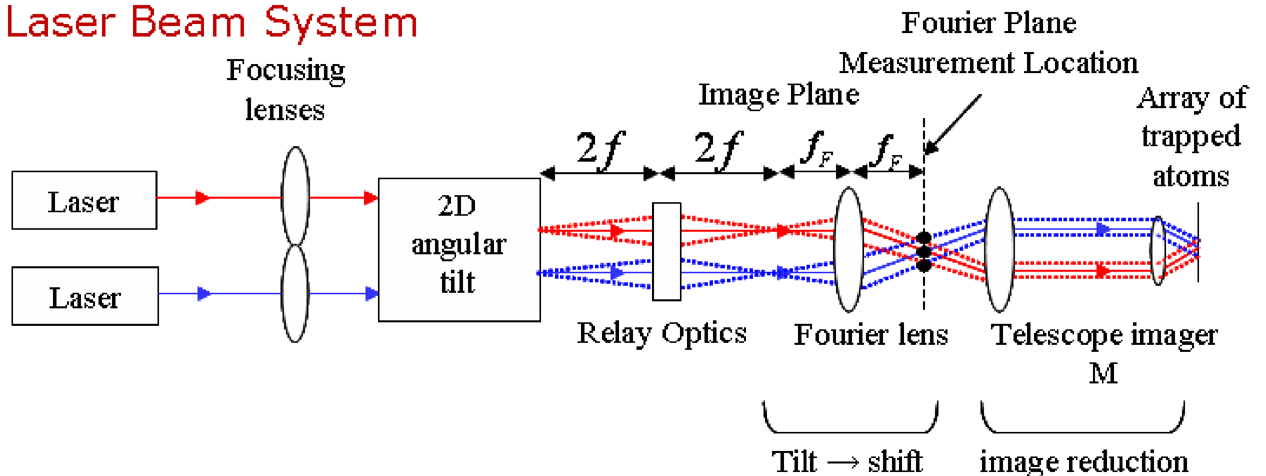

Figure 2 : MEMS Optical Beam Steering System. The tilt of the MEMS mirrors is translated into a lateral shift through an optical system, thus allowing the laser to address specific locations in a 2-D lattice. Source : C. Knoernschild, C. Kim, F. P. Lu and J. Kim, Multiplexed Broadband Beam Steering System utilizing High Speed MEMS Mirrors, Optics Express 17, pp 7233 (2009): http://arxiv.org/abs/0902.1574v1 (2009).

Mirror Design and Characterization

In order to understand and improve the mirror design, a lot of work has been put into thorough characterization of both mechanical and electrical properties of our mirrors. Basic characterization

includes DC and transient characterization, thermal, optical, and resonance analysis. In a DC analysis, we study tilt angle vs. actuation voltage and radius of curvature of the reflective plate using the Zygo optical interferometer. In a transient analysis, we measure the settling times of the mirrors with an optical position sensitive detector. Resonance analysis is also done with the PSD, primarily to evaluate the spring characteristics and compare the physical spring characteristicsx with the theoretical spring design. Thermal analyses are done to ensure optical quality over different input powers and temperatures, and optical analysis includes reflectivity measurements as well as radius of curvature analysis.

Thin Film Stresses

As mentioned previously, the reflective plates of the mirrors are coated in metal via evaporation to optimize reflectivity at the target wavelength. A thin layer of chromium is first evaporated to promote adhesion, followed by a thicker layer of the reflective metal. These thin films apply stresses on the substrate, and due to the thinness of the substrate (~3.5um), these stresses are enough to cause the mirror to curve. The stresses result from two primary sources: thermal and intrinsic stress[4]. Thermal stress occurs since the evaporation performed at higher than room temperature; upon cooling, the difference in thermal expansion of the two metals causes stress. However, at lower temperatures the intrinsic stress caused by the microstructure of the film dominates, and this is the effect that we will attempt to control. The deposition parameters that affect the stress are the film material, deposition temperature, deposition rate, deposition pressure, and film thickness.

One of my first projects was to characterize the thin film stresses for a silver coating. Since our two target wavelengths were 480nm and 780nm, gold would have been a sub-optimal choice from a reflectivity standpoint. Thus, we chose silver due to its high reflectivity at both wavelengths. By changing the deposition parameters, we were hoping to optimize a process to minimize the curvature of the mirror plate.

The parameters explored in this study were silver film thickness and chrome deposition rate. For the first experiment, the silver thickness was varied while the chrome parameters remained the same, thus allowing us to gauge the effects of silver thickness. Due to time constraints, we were not able to evaporate a large number of samples, so we opted to evaporate a few different thicknesses, including 80nm, 160nm, and 240nm of silver. The chrome used was 5nm thick, evaporated at 5Å/s. From Figure 3, it appears that the initial chromium deposition applies a tensile stress, and additional silver on top of the chromium tends to add compressive stress. However, as the silver film becomes thicker, the effect of additional silver becomes less pronounced.

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[4] Controlling Stress in Thin Films. FlipChips. http://www.flipchips.com/tutorial22.html

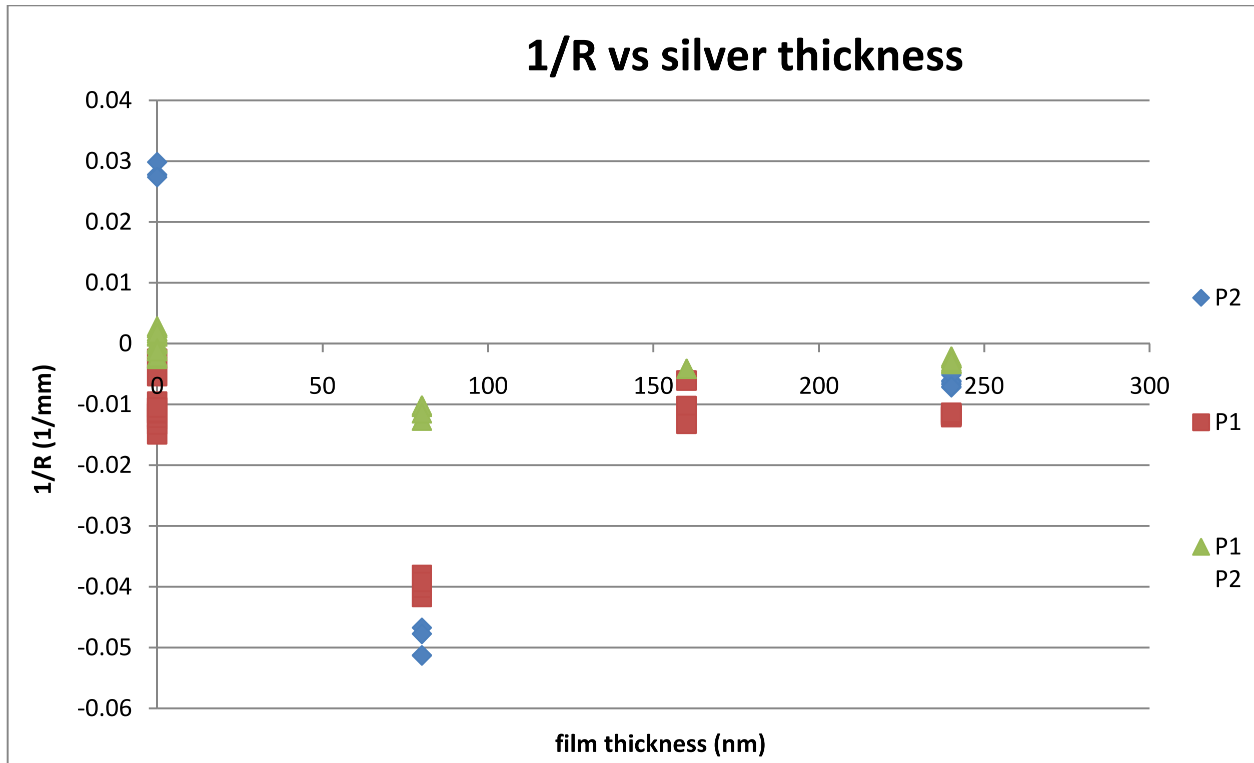

Figure 3 : Radius of Curvature vs Silver Film Thickness. P1 samples have a mirror plate with 2um thickness, P2 samples are 1.5um thick, and P1-P2 are 3.5um thick. The 0 measurement point is the initial radius of curvature, before any metal is deposited.

We also calculated film stress using Stoney's Equation. Stoney's Equation[5] for thin film stress ($\frac{1}{R} = \frac{6\, t_f\, \sigma}{E_{si}\, t_s^2}$) relates radius of curvature (R), film thickness (t_f), stress (σ), elastic modulus of the substrate (E_{si}), and substrate thickness (t_s). A plot of stress vs. silver thickness is shown in Figure 4. Though we cannot measure the effect of chrome alone due to its tendency to oxidize, we can infer the effect of silver on stress. One point to note is that our metal coatings can no longer be called thin films as the thickness approaches 200nm, and thus Stoney's Equation may not be a great approximation. What we do see is that the silver applies a compressive stress to the surface, though this effect decreases as the film becomes thicker. More importantly, the stress between different thicknesses of substrate shows characteristically similar trends, only differing by an offset. This offset can be fully explained by the differing initial radius of curvature, which is different between the three types of samples due to fabrication differences. What Stoney's equation tells us is that the stress applied by silver is consistent and controllable, and thus can be used to control curvature.

[5] S. Jin, H. Mavoori, J. Kim and V. A. Aksyuk, Control of microelectromechanical systems membrane curvature by silicon ion implantation, Applied Physics Letters 83, pp 2321-2323 (2003).

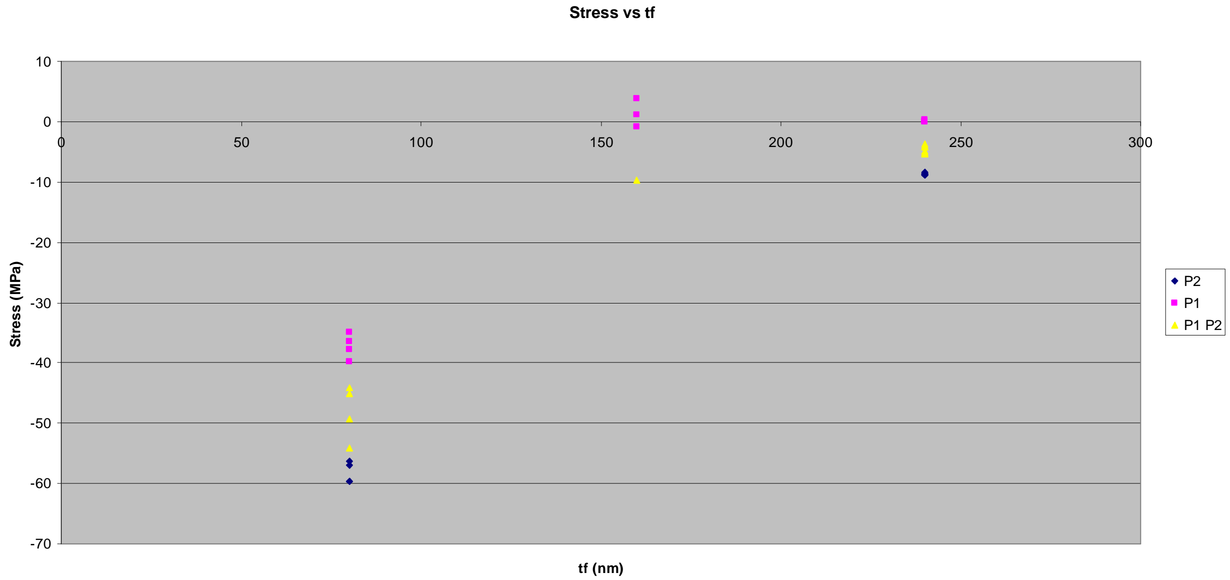

Figure 4 : Stress vs film thickness for Silver on polysilicon calculated from Stoney's Equation. Three different mirror designs are present in this graph which differ in mirror thickness: P1 has a 2um thick mirror, P2 is 1.5um thick, and P!-P2 is 3.5um thick.

Another important parameter is the deposition rate of the chrome layer. With a higher deposition rate, we expect the tensile stress to be greater due to the larger number of voids between atoms of the thin film[6]. Likewise, at lower deposition rates, we expect less stress. Comparing between two different deposition rates on two designs spanning multiple samples, we see in Figure 5 that a slower deposition rate does in fact reduce the tensile stress created by the chrome layer. All samples had the same silver deposition parameters and thus differed only in chrome deposition rate.

Though the number of data points is small, we can predict from all of this data the deposition parameters to minimize the stress on the mirror plate, given a mirror design and initial curvature.

DC Characterization and Mirror Design

DC Characterization is done with the Zygo optical interferometer. In the course of a DC characterization, we study tilt angle vs. actuation voltage, maximum controllable tilt angle (snapdown angle), and radus of curvature at each tilt angle. Snapdown angle determines the maximum lateral shift of our optical system, and thus is an extremely important parameter. Design parameters determine this snapdown angle, in particular electrode design and the gap between the substrate and mirror plate. Radius of curvature (RoC) is important for optical quality as mentioned previously, and it is important to note that the mirror plate deforms as it is tilted, due to the uneven application of the electrostatic force. Though we have design goals in mind when designing our mirrors, we can only verify these parameters via testing.

[6] Controlling Stress in Thin Films. FlipChips. http://www.flipchips.com/tutorial22.html

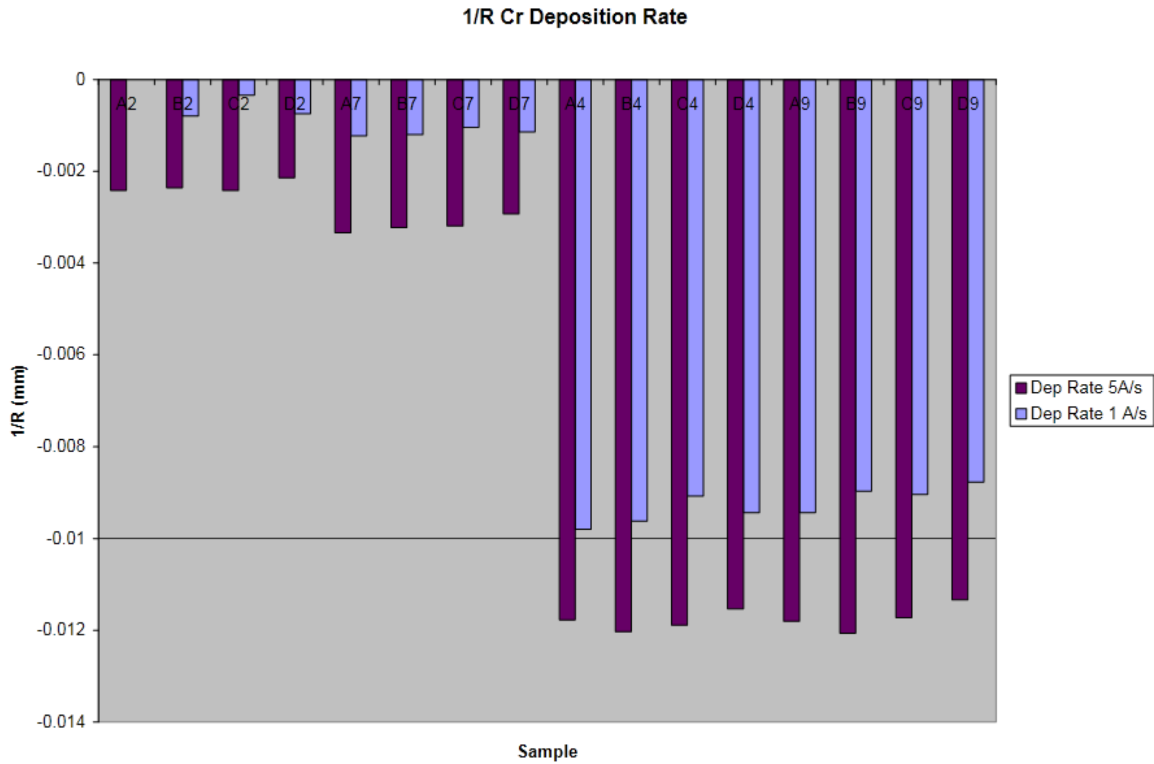

Figure 5 : Radius of curvature vs Cr deposition rate across two different mirror designs. By slowing down the deposition rate, we can reduce the initial tensile stress induced by the Cr adhesion layer.

Suspended Mirror Plates

Due to the deformation of the mirror plate when tilted, the optical quality of the MEMS system has a tendency to degrade as the beam is shifted. To solve this problem, a new design was explored, which consisted of two mirrors plates, an actuation plate and a reflective plate, anchored together at just two points. Since the majority of the induced curvature due to tilting is induced along the axis of rotation, the two anchor points are placed orthogonal to this axis.

poly1-poly2 stack (t=3.5um)

poly1-air-poly2 suspended plate

Figure 6 : Stacked mirror plate (left) vs suspended mirror plate (right)

Initial testing shows this design to be successful at preventing the transfer of deformation to the reflective plate; in Figure 8 is a measurement of a simple mirror plate, and in Figure 7 is a suspended

mirror plate of similar characteristics.

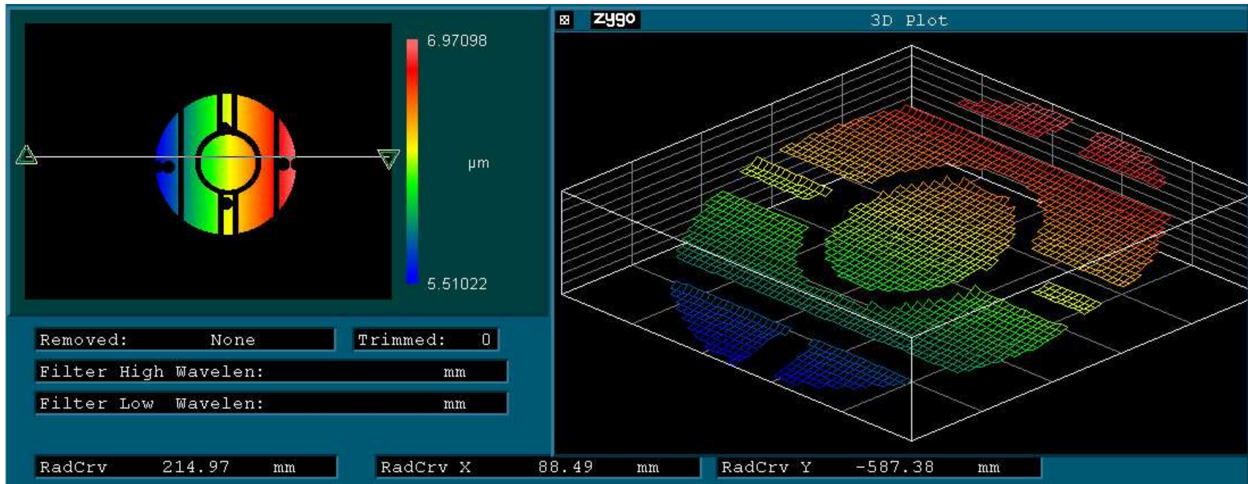

Figure 7 : Suspended mirror plate Zygo measurements at full tilt

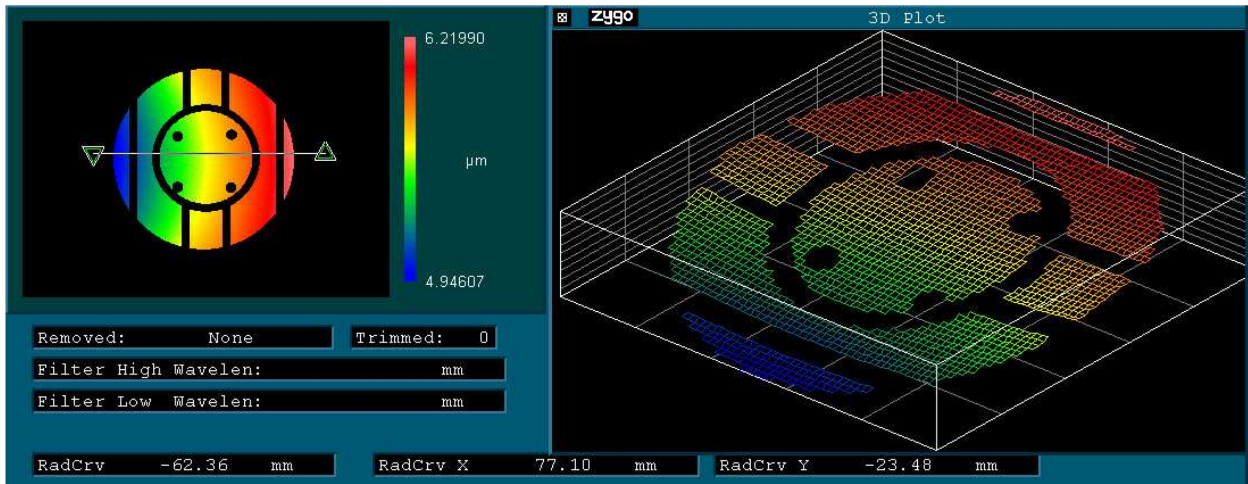

Figure 8 : Stacked mirror plate Zygo measurement at full tilt

In the stacked mirror plate, we see a radius of curvature of ~8cm along the axis of rotation (AoR), and -2.5cm orthogonal to the AoR. With the suspended plate design, the curvature along the AoR does not change, but the RoC orthogonal to the AoR becomes nearly flat, at ~60cm, a huge improvement.

Testing of all samples show this same trend, and thus this particular design has been successful in meeting our goals. However, work still needs to be done on optimizing transient characteristics and snapdown angle of this suspended plate design.

Transient Characterization and PSD

Transient data allows us to observe the behavior and settling times of the mirrors. Since one of our main goals for this MEMS system was to be able to switch locations as quickly as possible, speed is a significant design consideration. In order to do transient characterization, we use an optical position sensitive detector (PSD). The requirements for this PSD circuit are somewhat unique due to the fast

transients we would like to observe. As such, commercial products that meet these requirements do not satisfy all of our requirements, are extremely expensive, and hard to find. Thus, one of my projects was to fabricate a custom PSD based on a Hamamatsu S2044 photodiode, which promised settling times of about 0.3us. The goal for this custom circuit was to have faster than 1us resolution, high signal to noise ratio, and feedback to allow the user to tune the input power easily and quickly.

The S2044 photodiode has a four quadrant current output, one at each corner, which allows the user to convert its currents to a X and Y position via the following formulas:

(1) $X = \frac{(X2+Y1)-(X1+Y2)}{X1+X2+Y1+Y2}$

(2) $Y = \frac{(X2+Y2)-(X1+Y1)}{X1+X2+Y1+Y2}$

Basing my circuit off work by a previous student[7], I developed a board to convert the photodiode currents into voltages using a transimpedance stage, and perform the necessary circuit arithmetic to give the user X and Y positions. In addition, feedback was added in the form of a simple power meter, which outputted to a row of LEDs that represented the input power into the system, allowing the user to quickly and easily adjust the input power to optimize speed and sensitivity.

The transimpedance stage is based off the Texas Instruments OPA656[8] amplifiers, which is a high speed amplifier with great noise characteristics. Simple signal-to-noise ratio (SNR) calculations allow us to optimize speed vs SNR, since bandwidth is dependent on the gain and the gain-bandwidth product of the amplifier. From the SNR analysis (See Appendix A), 110Kohm was chosen as the transimpedance gain.

The arithmetic is accomplished using a series of summing and inverting amplifiers, and the final division is done via an analog divider. The part chosen was the Analog Devices AD734[9], primarily for its high speed (10MHz bandwidth). However, the bandwidth of the divider is dependent on its denominator input voltage, thus the need for feedback to allow the user the tune the input power. In both the X and Y circuits, the denominator input is simply the sum of all four photodiode currents, and thus this value is used to tune the input power.

Feedback is accomplished by reading the sum of the four input currents. A PIC microcontroller is used to convert this data and output to a row of LEDs notifying the user if the input power needs to be adjusted.

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[7] Previous work by Justin Migacz provided a foundation for the circuits used in this PSD implementation

[8] See http://focus.ti.com/lit/ds/symlink/opa656.pdf

[9] See http://www.analog.com/static/imported-files/data_sheets/AD734.pdf

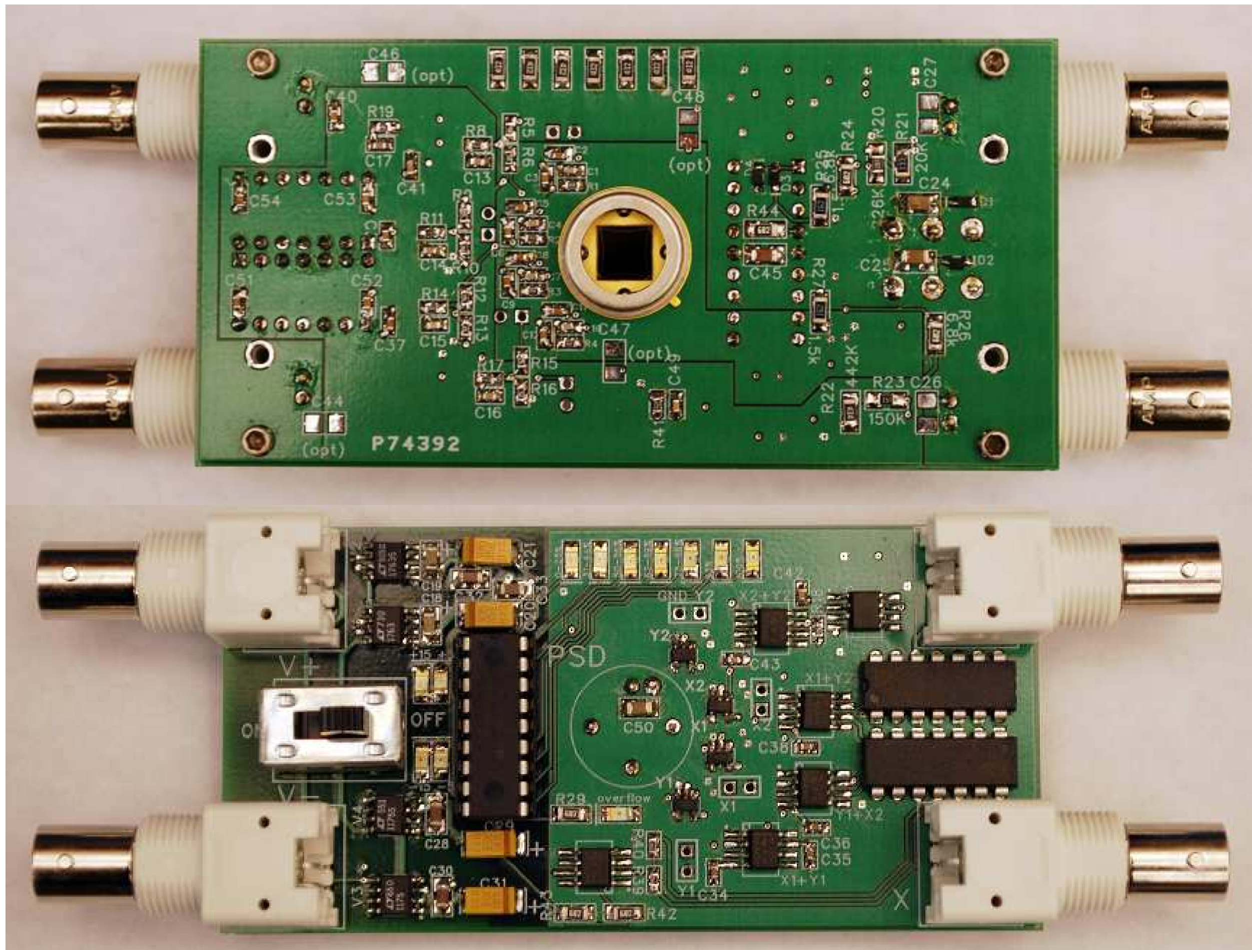

Figure 9 : PSD circuit after assembly

This project was successful in meeting all its goals. Shown in Figure 10 is a typical underdamped mirror transient, which the PSD is able to resolve fully. Though we did not deem it worthwhile to fully characterize its response, this PSD does surpass our original design goals.

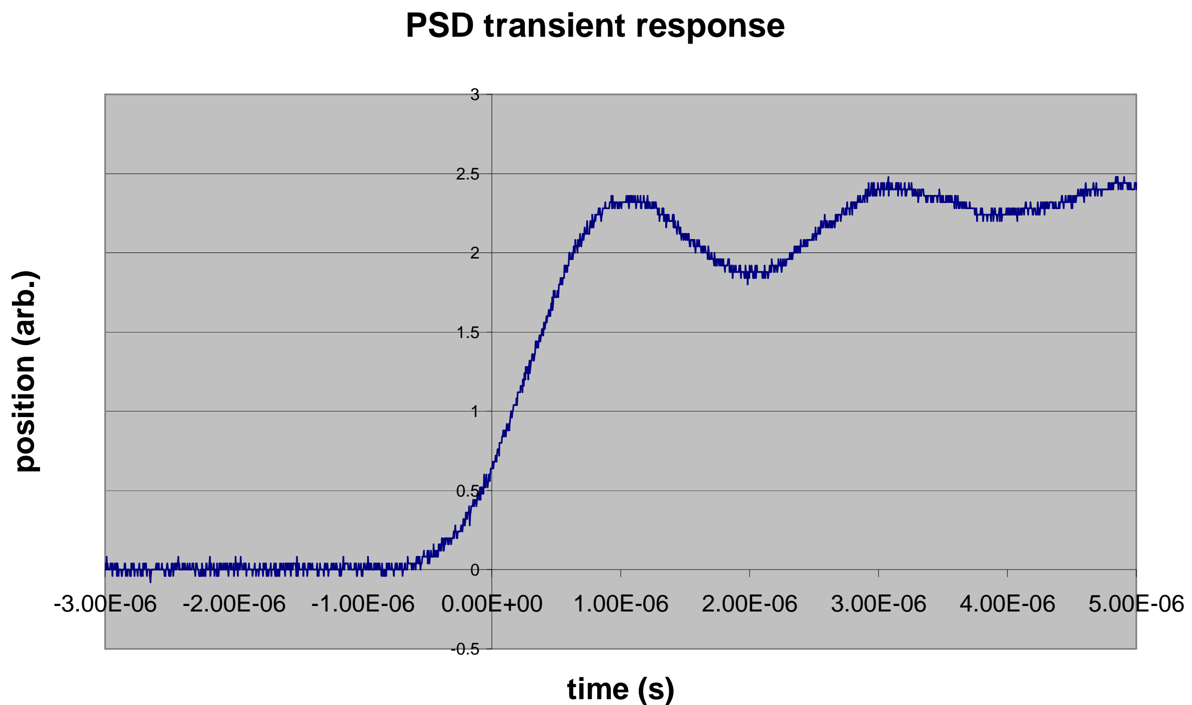

Figure 10 : typical PSD transient response. This waveform is a measurement of an underdamped mirror, though the response speed is still limited by the physical characteristics of the mirror itself and not the PSD.

Mirror Control Electronics

The electronics for the MEMS system are quite specialized, particularly due to the high actuation voltages and fast speeds required. At the end of summer 2009, we set out a specification for a complete control system capable of meeting our requirements. These requirements were (1) the ability to interface with a computer for user input; (2) ability to switch a 10 beam system in under 5us; and (3) modularity to allow for the user to balance cost and performance.

Amplifiers

Given the high voltage required (up to 200V), the first step was to find a way to deliver those voltages in a precise and highly controllable manner. High voltage amplifiers capable of the voltage required as well as 1us settling time turned out to be difficult to find; only a single manufacturer, Apex Electronics (now owned by Cirrus Logic, Inc), offered amplifiers that met our requirements.

Apex had a number of parts that we considered for our application, ranging from the low cost PA79 to the ultra-high speed PA94. Initially, the PA79[10] was considered for its low cost; at $65 for two channels, this chip is by far the cheapest option available to us. However, at best, the settling times are 5-8us to 150V. Two other options, the Apex PA84S[11] and Apex PA94[12], are both faster, but more expensive. The

[10] See http://www.cirrus.com/en/pubs/proDatasheet/PA79U_B.pdf
[11] See http://www0.cirrus.com/en/pubs/proDatasheet/PA84U_P.pdf

PA84S settles in 1us to 150V, while the PA94 is even faster, settling to 150V in 500ns. However, both parts are more expensive at $240 for a single channel, consume more power, and require heatsinking. The tradeoff between power, cost, and speed is a decision ultimately up to the end user, who will have a choice of amplifiers depending on the application (see System Integration).

Control System

The control system must have at least 40 channels in order to satisfy the 10 beam requirement (2 mirrors per beam, 2 electrodes per mirror). Due to the high channel count and high speeds required, I chose an FPGA based implementation that outputs to an array of high speed, high precision digital-to-analog converters (DACs). In order to provide user control, the system interfaces with a computer via USB 2.0. In Figure 11, a block diagram of the system is shown.

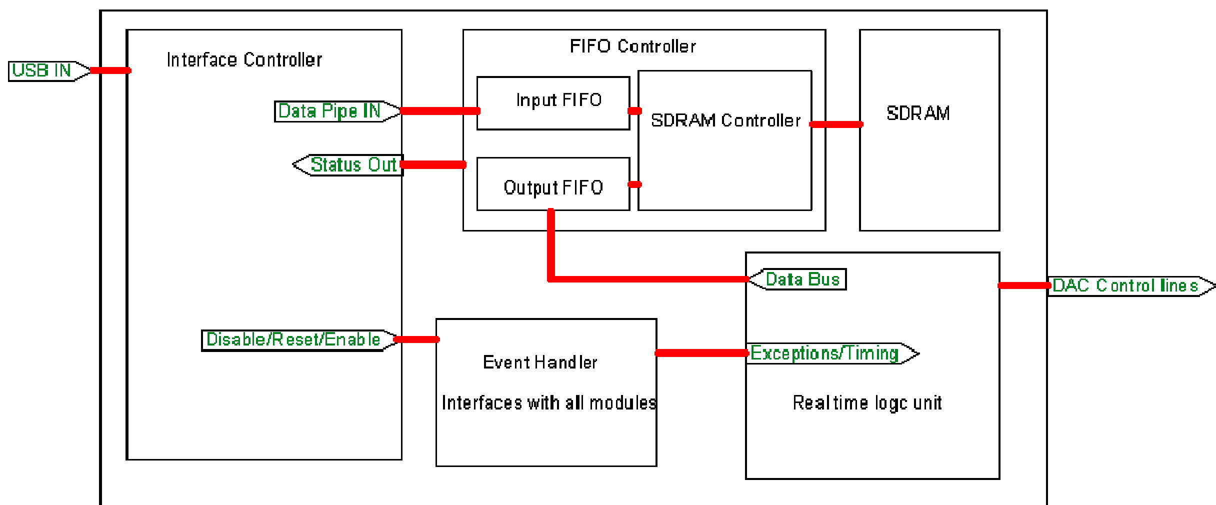

Figure 11 : MEMS Control System Block Diagram

Choosing an interface for the controller and computer was the first step of the process. Due to the bandwidth required, only a few options were viable. USB1.1 is widely available and easily implemented, but too slow. PCI has more than enough bandwidth, but the driver development cost is prohibitive and the interface is not plug and play compatible. Ethernet is one possibility, but it does not allow for the ease of plug and play that other interfaces provide. USB2.0 was chosen due to its plug and play nature, satisfactory bandwidth, and ease of software development. I chose an Opal Kelly XEM3005[13] FPGA board, which contains a Xilinx Spartan 3E FPGA, a Cypress USB2.0 interface chip, and 32MB of SDRAM onboard. Opal Kelly's solution was chosen because of the level of development tools provided; the majority of the USB to FPGA interface is provided by Opal Kelly, thus reducing development time substantially.

[12] See http://www.cirrus.com/en/pubs/proDatasheet/PA94U_M.pdf
[13] See http://www.opalkelly.com/library/XEM3005-UM.pdf

Figure 12 : Opal Kelly XEM3005 FPGA Board. Model provided by Opal Kelly and rendered in Solidworks Photoworks.

Next, a DAC chip had to be chosen. The requirements were a settling time of less than 1us and at least 14 bits of resolution with <1LSB of integral nonlinearity or 16 bits of resolution with <4LSB of INL. Due to the speed constraint, only parallel bus DACs were suitable. After careful consideration, the AD5557[14] from Analog Devices was chosen. The AD5557 has two current output DACs in one package, 14 bits of resolution, 0.5us settling time, and <1LSB of INL. All parameters were verified in testing, where our sample showed INL of <0.8LSB across the full range of the DAC and settling time of <500ns when coupled with an Analog Devices AD8655[15] amplifier to convert to a voltage output. Each DAC channel on the chip has a separate input and output register, which allows for the input register to be set without the output of the DAC changing. These registers allow for the user to set multiple DACs in sequence, yet update their outputs simultaneously.

The FPGA control logic was developed with streaming data in mind. Modern operating systems have latencies on the millisecond scale, which is much too slow for our system to run in real time. As a result, the operating scheme chosen involves the user buffering data from the computer onto the FPGA though the 32MB SDRAM. Due to the nature of SDRAM, this memory is most efficiently written and read in pages. Thus, the SDRAM FIFO makes us of an input and output buffer, allowing for values to be written and read individually without compromising the performance of the system. The SDRAM controller automatically moves data from the input buffer on the USB side to the SDRAM, and also automatically moves data from the SDRAM to the output buffer that is read by the control logic. The SDRAM fill status is constantly monitored and sent back to the computer to prevent the buffer from being overrun.

The control unit itself reads data from the SDRAM output buffer and executes commands based on the data. The control until has four commands that it implements at the moment: (1) load a DAC input register specified by an address; (2) update the output of all DACs; (3) delay by a specified number of

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[14] See http://www.analog.com/static/imported-files/data_sheets/AD5547_5557.pdf

[15] See http://www.analog.com/static/imported-files/Data_Sheets/AD8655_8656.pdf

clock cycles; (4) delay until externally triggered. The external trigger delay allows for the system to be easily synchronized with an outside clock source.

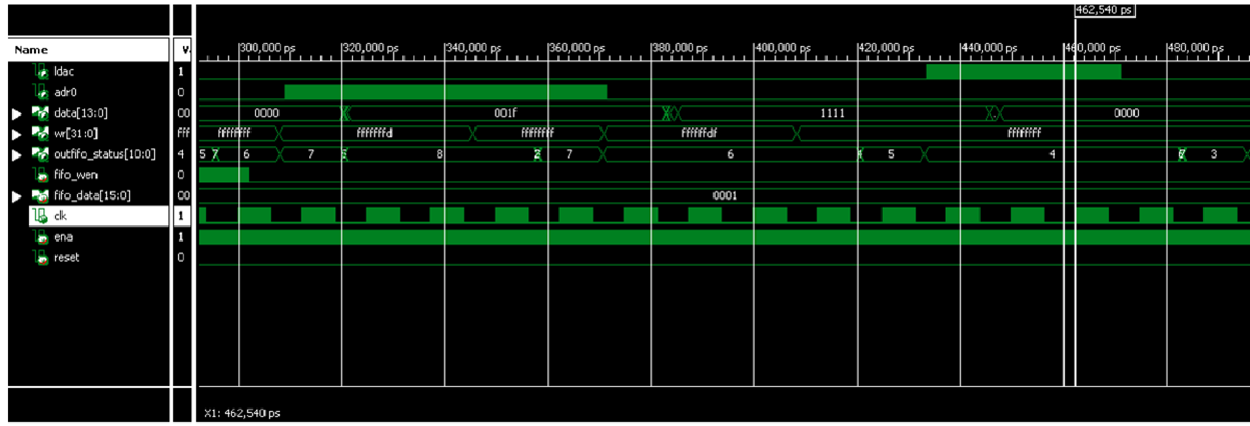

Figure 13 : Simulation of the logic control. The control unit sets the DAC by pulsing WR low, and updates the DAC output by pulsing LDAC high.

The system is designed for a 66MHz clock provided by a PLL on the Opal Kelly board. At this speed, the system can update and set all 40 channels in 3.2us, well within the 5us constraint. In Figure 14 is an arbitrary time waveform of a single channel, taken at the output of the DAC to show functionality.

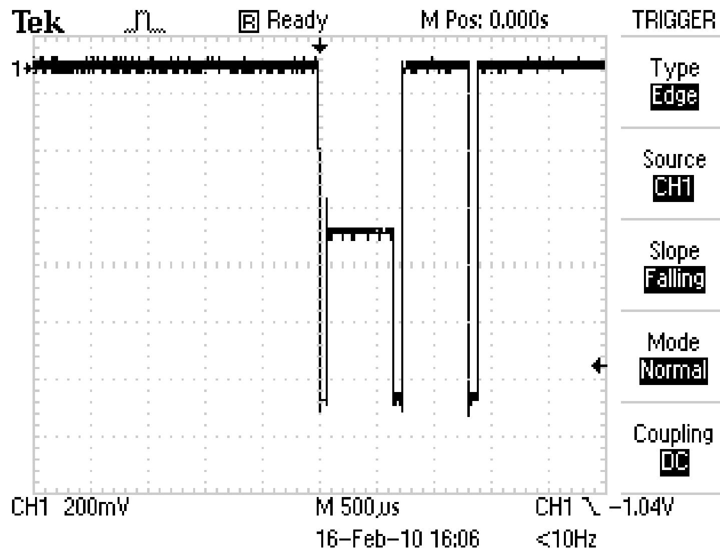

Figure 14 : Example arbitrary time based waveform for one channel generated by MEMS controller. Output is taken at the output of the DAC

System Integration

The complete control system consists of the FPGA board, DACs, and amplifiers. In order to make the system modular, the full system consists of multiple parts. The Opal Kelly FPGA board connects to a motherboard, which connects the different parts of the system. Separate boards contain the DACs and amplifiers. Each DAC board contains 8 DAC channels, and up to 5 DAC boards can connect to the

motherboard. The DAC boards are addressed in physical order, i.e. the leftmost DAC board contains channels 0-7, the next one contains channels 8-15, etc.

The amplifier board stacks on top of a DAC board and contains amplifiers for 8 channels as well. Because of the amplifier choices, two different boards will be available, one for the PA79 and one for the PA94. The outputs of the amplifier boards can either be used directly or routed to a breakout board for usage with different connectors. Shown in Figure 15 is a rendering of the physical design. The Opal Kelly board is on the left side, and there are five DAC boards in the rendering. The leftmost DAC board has an amplifier board on top of it.

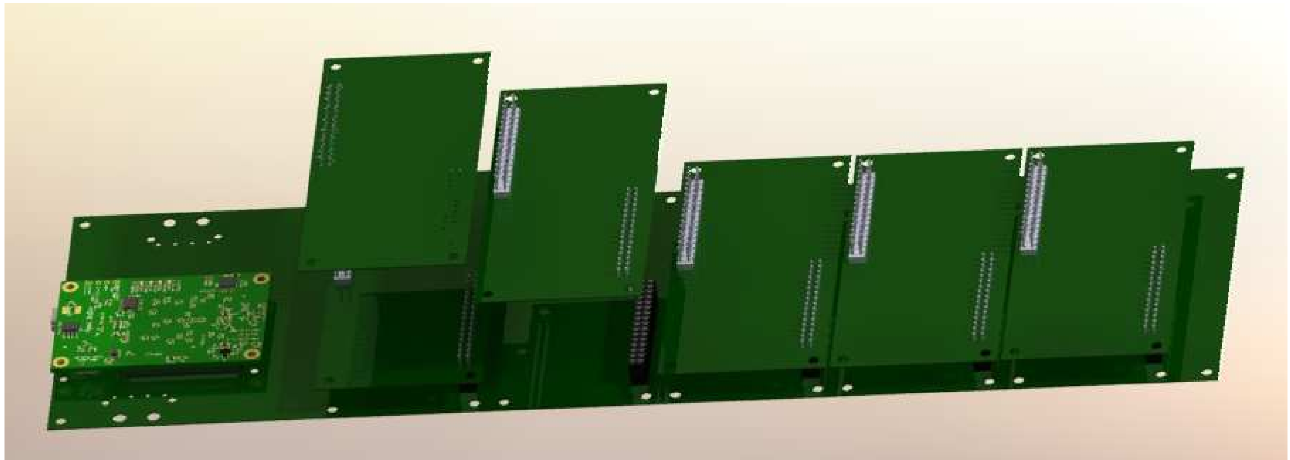

Figure 15 : MEMS Controller system physical layout. The FPGA board is on the left, and there are five DAC boards that can be attached to the system, thus allowing for both modularity and scalability.

Conclusion and Future Work

This MEMS optical beam steering project has made large strides forward in the time that I've been here, and I'm glad to have been part of the effort. Through the testing and optical design phase, I helped collect and analyze data to help improve our mirror designs, where I learned about optical setups, mirror fabrication, and in building the PSD circuit, I obtained a great deal of experience in circuit design, PCB design, and assembly.

After these smaller projects, I took on the control electronics as my major project. Starting with a set of design goals, I created a system that exceeded those requirements, and while doing so, exposed myself to all sorts of electronics, including digital design with the FPGA, high voltage and high speed electronics, system integration, PCB design, and much more along the way. Though we are at the final stages of this project, there still lies more to be done in the future, including assembly of the system, followed by a full characterization. The PA94 amplifier boards have not been designed yet, which presents a whole new set of challenges; however, the foundation is in place now and is ready to be built upon.

Not only has my undergraduate research experience been exciting, but it has helped me develop as an engineer as well. I am thankful to have had the opportunity to participate in this research project.

Acknowledgements

I would like to thank Dr. Jungsang Kim, Caleb Knoernschild, and Dr. Felix Lu for giving me the opportunity to work with them on such a novel project, and for their constant support throughout the course of the project. They have been wonderful to work with and I could not have come this far without them. I would also like to thank Dean Martha Absher and the Pratt Fellows program for the opportunity to participate in a high level, continuous multi-semester research project.

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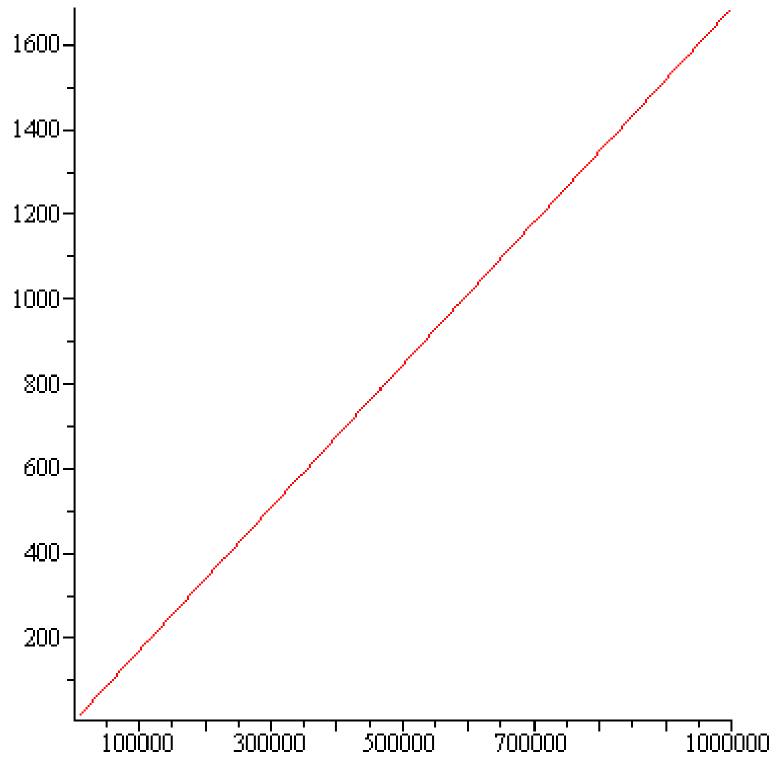
Appendix A: SNR Calculations for PSD transimpedance stage

```
> SNR:=(Is,Rf)->Is^2*Rf^2/((2*q*Is*Rf^2+4*kb*T*Rf+In^2*Rf^2)*B);
```

$$SNR := (Is, Rf) \rightarrow \frac{Is^2\ Rf^2}{\left(2\ q\ Is\ Rf^2 + 4\ kb\ \ T\ Rf + In^2\ Rf^2\right)\ B}$$

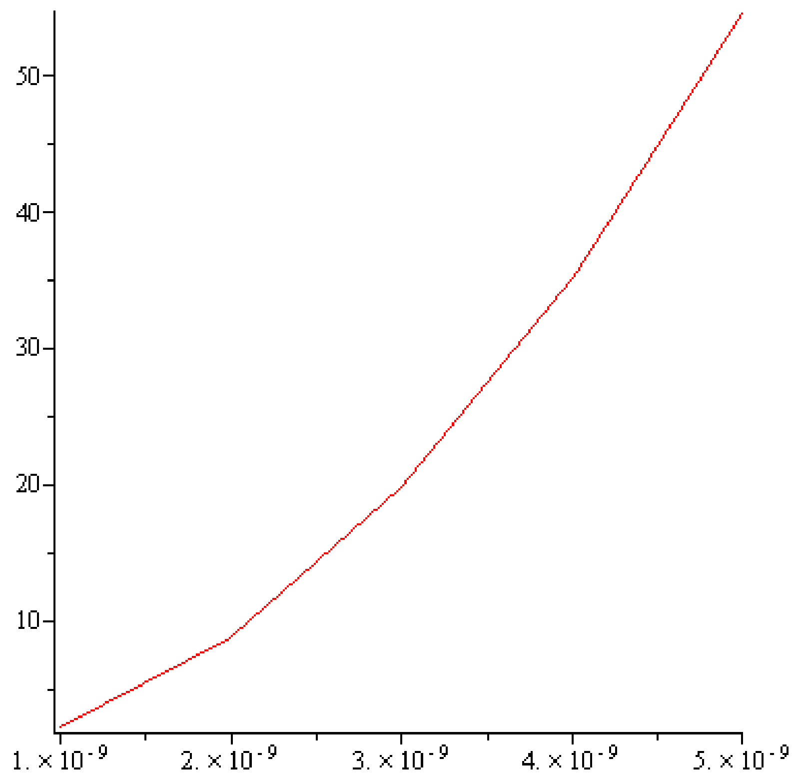
The signal to noise ratio (SNR) for a transimpedance amplifier is determined by the ratio of signal power to noise power. This analysis takes into account noise sources including shot noise, thermal noise from the feedback resistor, and amplifier current input noise.

```
> q:=1.60217653e-19:
> kb:=1.3806505e-23:
> B:=3e6:
> Is:=1e-6:
> In:=1.3e-15:
> T:=300:
> plot([seq([Rf,SNR(10e-9,Rf)],Rf=10000..1000000,1000)]);
```



At a 10nA input current, the SNR is reasonable for transimpedance gains over 100,000.

```
> plot([seq([Is,SNR(Is,110000)],Is=1e-9..5e-9,1e-9)]);
```



Choosing 110,000 ohm as the feedback resistance, above is a plot of SNR vs input current. From this plot, we can see that this transimpedance stage should be able to resolve currents down to ~1nA.

```
> solve(SNR(x,110000)=1,x);
>
```

$$6.726819291 \, 10^{-10}, \; -6.717206232 \, 10^{-10}$$

```
>
```

At a transimpedance gain of 110,000, the SNR approaches 1 as the current approaches 0.7nA. This value for the transimpedance gain provides a good balance between speed and SNR, especially since the input current should be on the order of 1uA.